PATENTPULSE AI · DAILY PATENT ALPHA

Sample Brief: AI infrastructure

October 20, 2026 · 4 newly published USPTO applications, ranked by Signal Score

Real USPTO applications published in the last 60 days. Analysis is AI-generated opinion, not legal or investment advice.

AT A GLANCE



#2 **Parallel MAC circuit with context memory**

Watch competitor · SEMICONDUCTOR ENERGY…



#3 **Configurable sum-compare adder trees for NN**

Early-stage bet · Fotonation Limited



#4 **NN Pipeline Resource Prediction**

Watch competitor · PAYPAL, INC.

TOP PICK



#1 Compiler graph fusion for neural nets

NEURAL NETWORK LAYER FUSION

Watch competitor | **AI** | **#1 of 100 screened in sample window**

Applicant: NVIDIA Corporation • **Inventor:** Bin Fan +3 • **Entity:** Regular Undiscounted • **CPC:** G06F 8/4441, G06F 8/451, G06F 9/5038 +4

Pub. No. US20260319775A1 • App. No. 19313509 • Filed 2025-08-28 • Published 2026-10-15



Broad compiler fusion claims; NVIDIA applicant; no commercialization details in record.

WHY THIS ONE STANDS OUT

The problem it solves: Selecting node combinations in a graph by calculated cost values to generate fused code.

Who would pay for it: potentially AI hardware vendors seeking compiler differentiation.

Likely buyers & why: AMD: exposure if ROCm uses cost-driven fusion; Google: TPU compiler risk; Qualcomm: edge NN compiler overlap

What makes it hard to copy: Easy to copy by using different cost metrics or selection criteria outside the exact claim language.

WHAT TO DO NEXT

1. IP counsel: run targeted prior-art search on cost-based graph fusion in compilers
2. VC analyst: map continuation family to NVIDIA product compilers

View USPTO publication (PDF) →

Source: USPTO Open Data Portal (published applications). Scores and analysis generated by Grok. Not legal or investment advice.

THE FULL RANKING

PatentPulse Signal Score (0–100): market pull 25% · acquisition interest 25% · defensibility 20% · innovation 15% · timing 15%, each scored by Grok from the application's abstract and independent claims. Honest absolute scale: a typical published application scores lower; 65+ is strong; 75+ is exceptional. Published applications are not granted patents; claims may change.



#2 Parallel MAC circuit with context memory

OPERATION CIRCUIT, SEMICONDUCTOR DEVICE, AND ELECTRONIC DEVICE

Watch competitor | AI | #2 of 100 screened in sample window

Applicant: SEMICONDUCTOR ENERGY LABORATORY CO., LTD. • **Inventor:** Munehiro KOZUMA +3 • **Entity:** Regular Undiscounted • **CPC:** G06F 7/523, G06F 7/5443, G06N 3/048 +16

Pub. No. US20260319746A1 • App. No. 19718209 • Filed 2026-06-24 • Published 2026-10-15



Neural-net product-sum circuit; no market or timing data in record.

WHY THIS ONE STANDS OUT

The problem it solves: Signal delay in parallel product-sum operations for neural nets.

Likely buyers & why: Companies filing in G06N 3/045: potential FTO issue if claims survive

What makes it hard to copy: Easy to copy by altering register ordering or memory access.

WHAT TO DO NEXT

1. Review full specification and drawings for unclaimed embodiments
2. Search CPC G06F 7/523 and G06N 3/045 for same-day publications

Key risks: Continuation status may narrow claims; No commercialization details in record • **Alice/§101:** Medium – claim 1 recites concrete circuit connections but ties to abstract neural-net math

View USPTO publication (PDF) →

Source: USPTO Open Data Portal (published applications). Scores and analysis generated by Grok. Not legal or investment advice.



#3 Configurable sum-compare adder trees for NN

PROCESSING ELEMENT FOR A NEURAL NETWORK

Early-stage bet | AI | #3 of 100 screened in sample window

Applicant: Fotonation Limited • **Inventor:** Mihai Munteanu • **Entity:** Small • **CPC:** G06N 3/063, G06N 3/048, G06N 3/045 +1

Pub. No. US20260320368A1 • App. No. 19553890 • Filed 2026-03-02 • Published 2026-10-15



Narrow configurable adder trees; small entity; dates and claims limit visibility

WHY THIS ONE STANDS OUT

The problem it solves: Configurable adder units for sum or comparison in tree layers

What makes it hard to copy: Easy to copy by using fixed non-multiplexed trees

WHAT TO DO NEXT

1. Search full file history for cited references
2. Map claim 1 elements to existing NN hardware

Key risks: Claims truncated and may narrow; Single inventor, small entity • **Alice/§101:** Medium – functional language on adder trees may invite §101

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Source: USPTO Open Data Portal (published applications). Scores and analysis generated by Grok. Not legal or investment advice.



#4 NN Pipeline Resource Prediction

INTELLIGENT ORCHESTRATION OF PROCESSING RESOURCES FOR PIPELINES

Watch competitor | AI | #4 of 100 screened in sample window

Applicant: PAYPAL, INC. • **Inventor:** Song Qiu +1 • **Entity:** Regular Undiscounted • **CPC:** G06F 9/3836, G06F 9/5038, G06F 9/46 +14

Pub. No. US20260319854A1 • App. No. 18873044 • Filed 2024-12-09 • Published 2026-10-15



Ordinary continuation claims on NN resource prediction; no unique details in record

WHY THIS ONE STANDS OUT

The problem it solves: Predicting resources to fulfill pipeline requests using historical and scheduled data

Who would pay for it: Operators of large computing pipelines

What makes it hard to copy: Easy to copy by substituting non-neural prediction methods

WHAT TO DO NEXT

1. Search cited prior art for the neural network limitation
2. Compare independent claims 1, 10, and 16 for differences

Key risks: Alice §101 rejection on abstract orchestration; Continuation may narrow claims further • **Alice/§101:** High – claims recite abstract idea of resource allocation implemented via generic NN

View USPTO publication (PDF) →

Pick to Act On: diligence plan

One-page plan for the top-ranked application in this brief.

What it claims	Compiler identifies node sets in graph, scores combinations by cost, picks set to fuse, emits code for combined function.
For investors	Standard compiler optimization reframed for graphs; value depends on unshown prosecution and prior art.
For IP counsel	Claims appear broad on cost-based selection; design-around likely via different cost metrics or node grouping rules.
Alice / §101 risk	High – claims recite generic compiler steps on abstract graphs without specific hardware tie-in
Acquirers to watch	• AMD: would need license if using similar graph fusion in ROCm compilers • Google: potential block on TPU compiler optimizations • Intel: exposure in oneAPI NN graph passes

DILIGENCE CHECKLIST (3–5 DAYS)

1. Does the full spec disclose specific cost functions or heuristics?
2. Any examples tying claims to measured speedups on real hardware?
3. Search results for similar cost-based fusion in prior NVIDIA or competitor patents?
4. What is the priority date, and how many independent claims are likely to survive Alice/Mayo analysis?
5. Are continuation or divisional applications pending?
6. What is the filing footprint beyond the USPTO (PCT, EP, CN, JP)?

KEY RISKS

- Continuation may narrow claims further
- Alice risk on abstract compiler steps
- Prior art density in graph partitioning

PLAYBOOK BY ROLE

VCs / founders: identify the assignee; if it is a startup, explore licensing or an early investment conversation.

IP counsel: pull the published claims and file wrapper; assess freedom-to-operate and continuation strategy.

Strategic buyers: add to the watchlist and track prosecution; claims may change before grant.

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